FIG.1

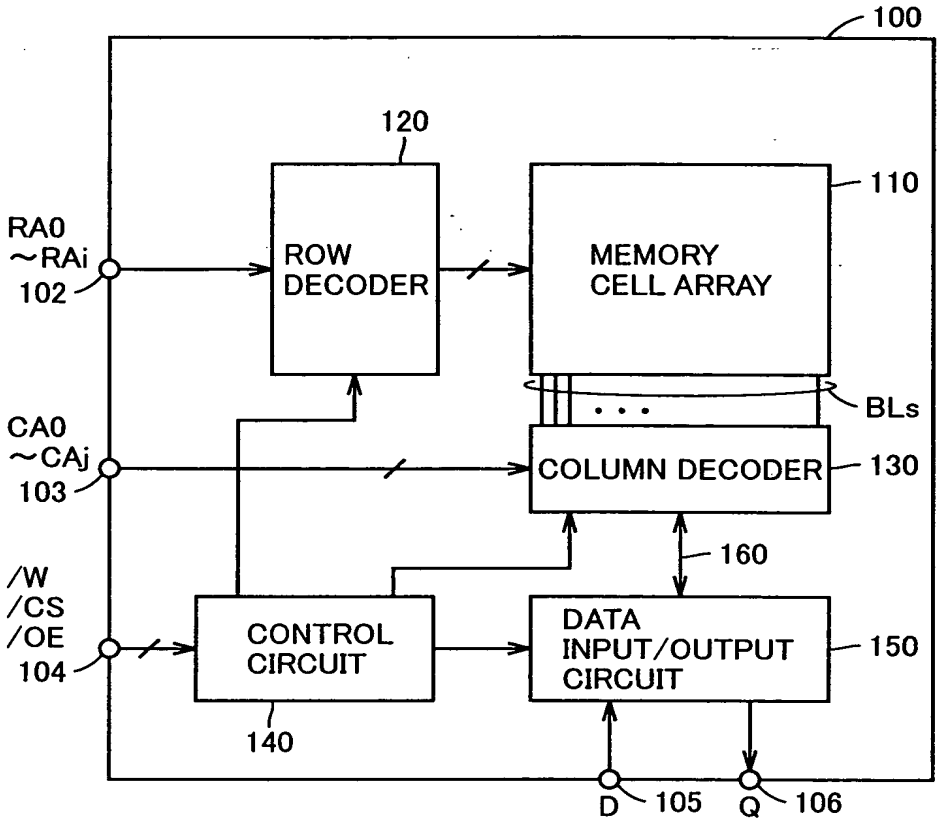
100
120
110
RA0
~RAi
102
ROW
DECODER
MEMORY
CELL ARRAY
BLs
CA0
~CAj
103
COLUMN DECODER
130
160
/W
/CS
/OE
104
CONTROL
CIRCUIT
DATA
INPUT/OUTPUT
CIRCUIT
150
140
D
105
Q
106

FIG.2

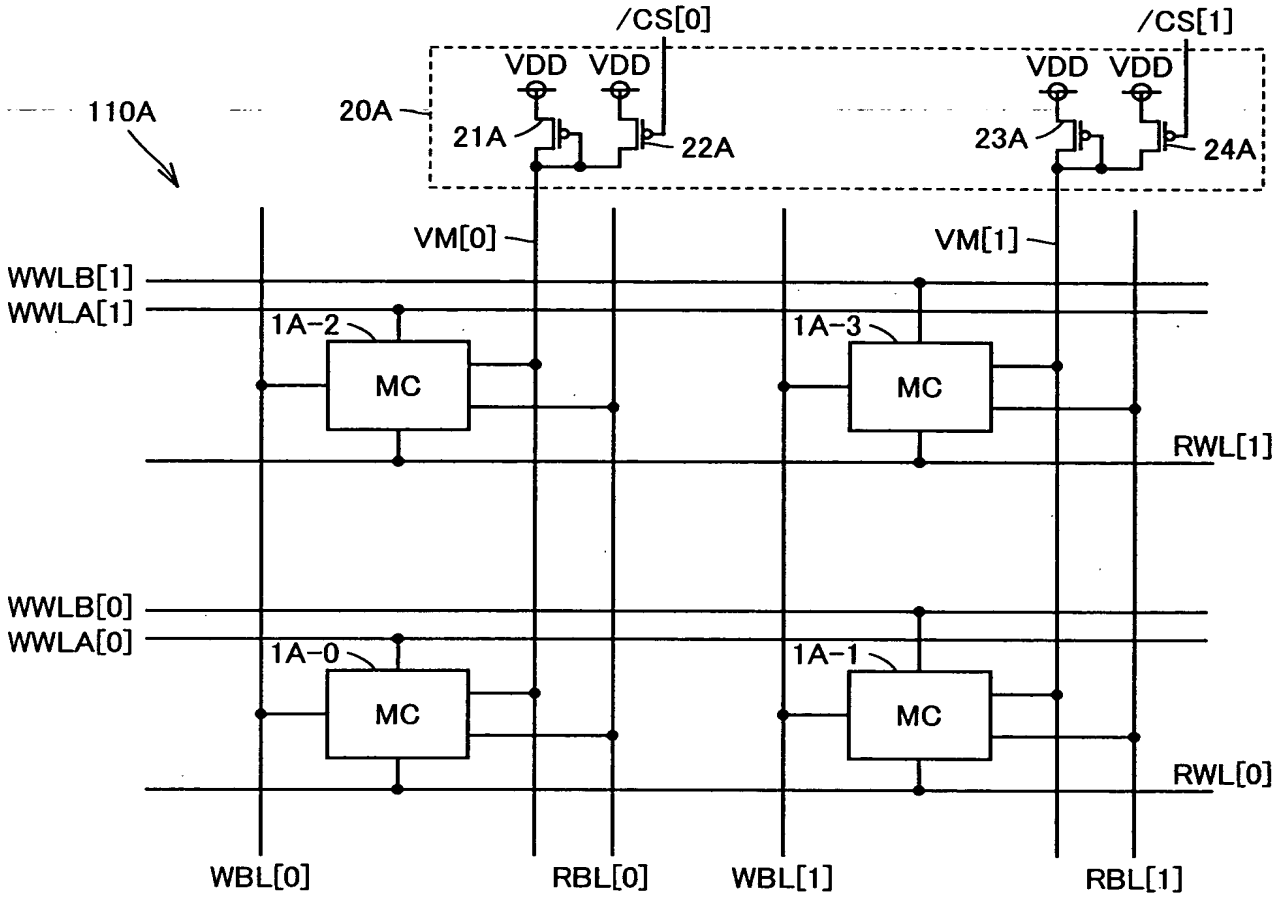
/CS[0]
/CS[1]
VDD
VDD
VDD
VDD
110A
20A
21A
22A
23A
24A
VM[0]
VM[1]
WWLB[1]
WWLA[1]
1A-2
1A-3
MC
MC
RWL[1]
WWLB[0]
WWLA[0]
1A-0
1A-1
MC
MC
RWL[0]
WBL[0]
RBL[0]
WBL[1]
RBL[1]

FIG.3

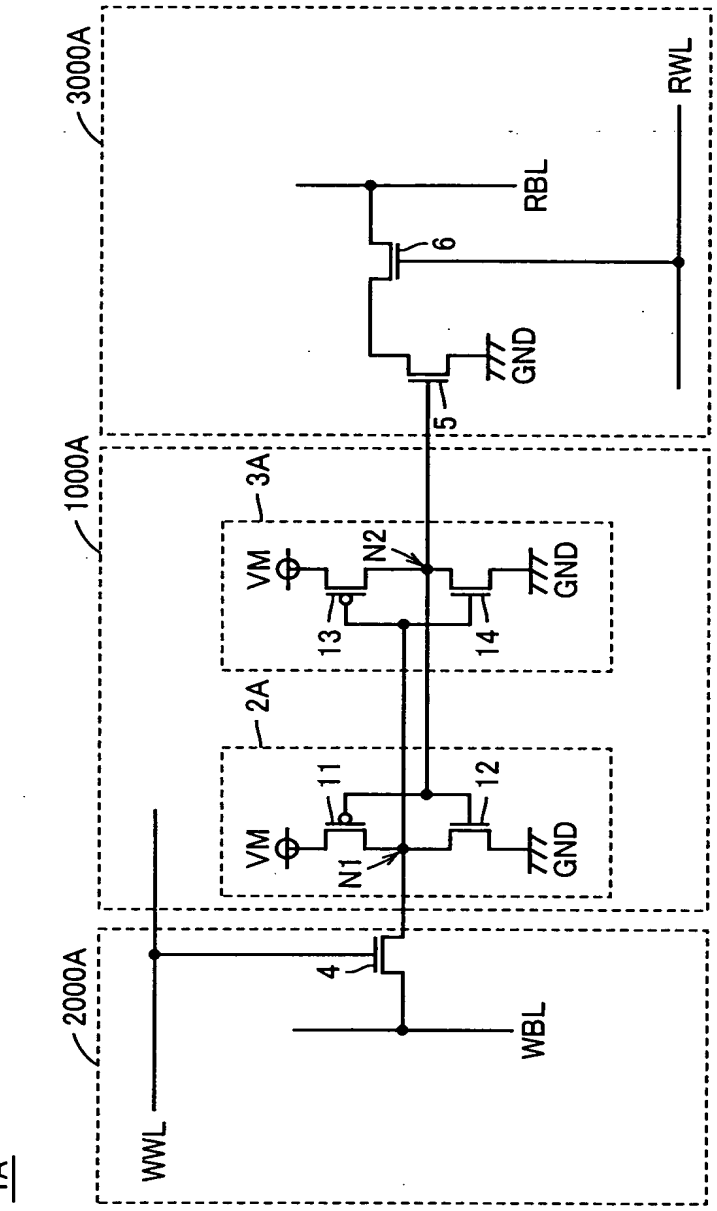
1A
3000A
1000A
2000A
3A
2A
RWL
RBL
WBL
WWL
GND
VM
N1
N2
4
5
6
11
12
13
14

FIG.4

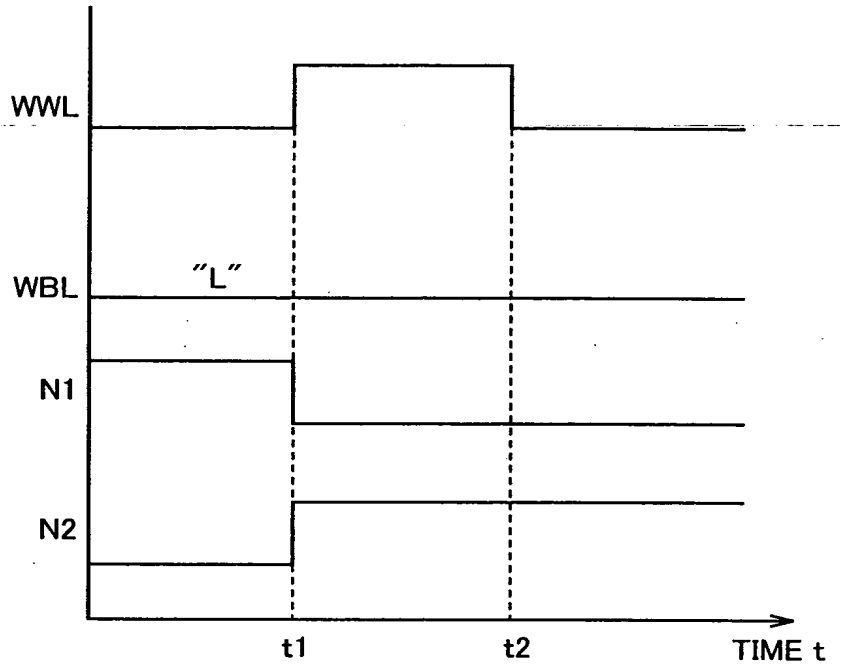

FIG.5

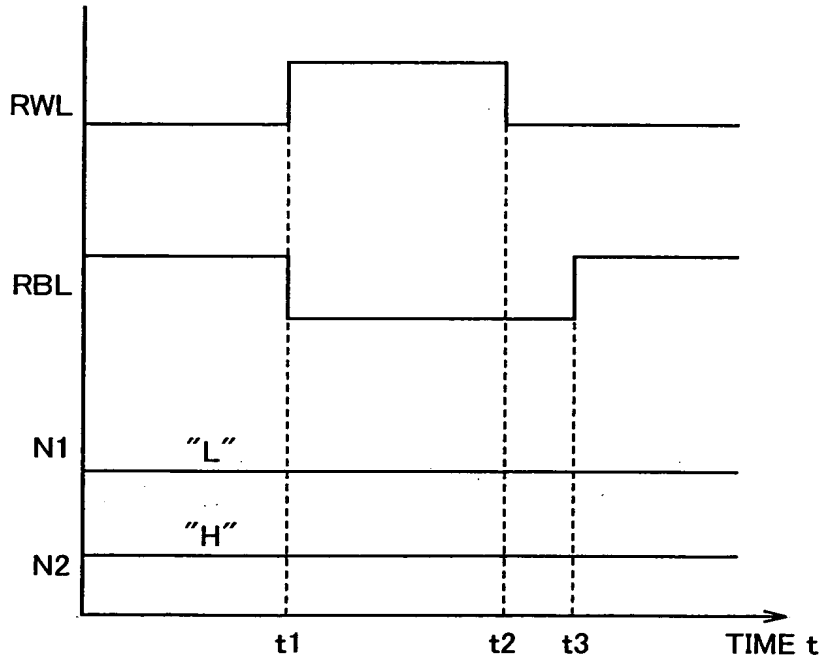

FIG.6

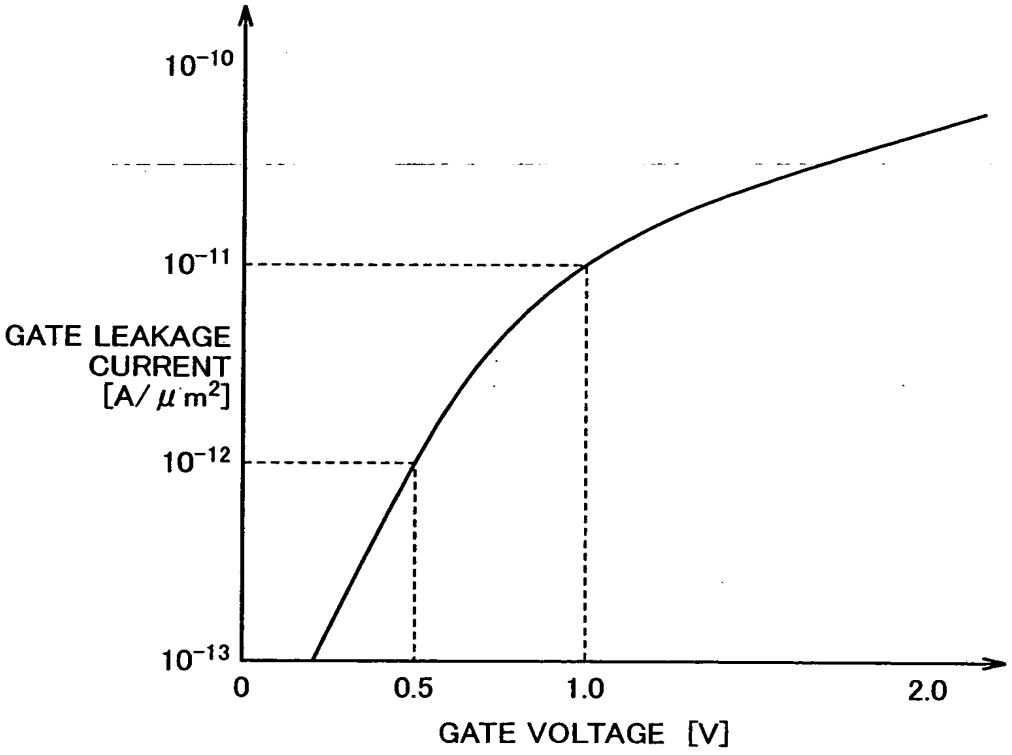
10^{-10}
10^{-11}
10^{-12}
10^{-13}
GATE LEAKAGE CURRENT [A/μm²]
0
0.5
1.0
2.0
GATE VOLTAGE [V]

FIG.7

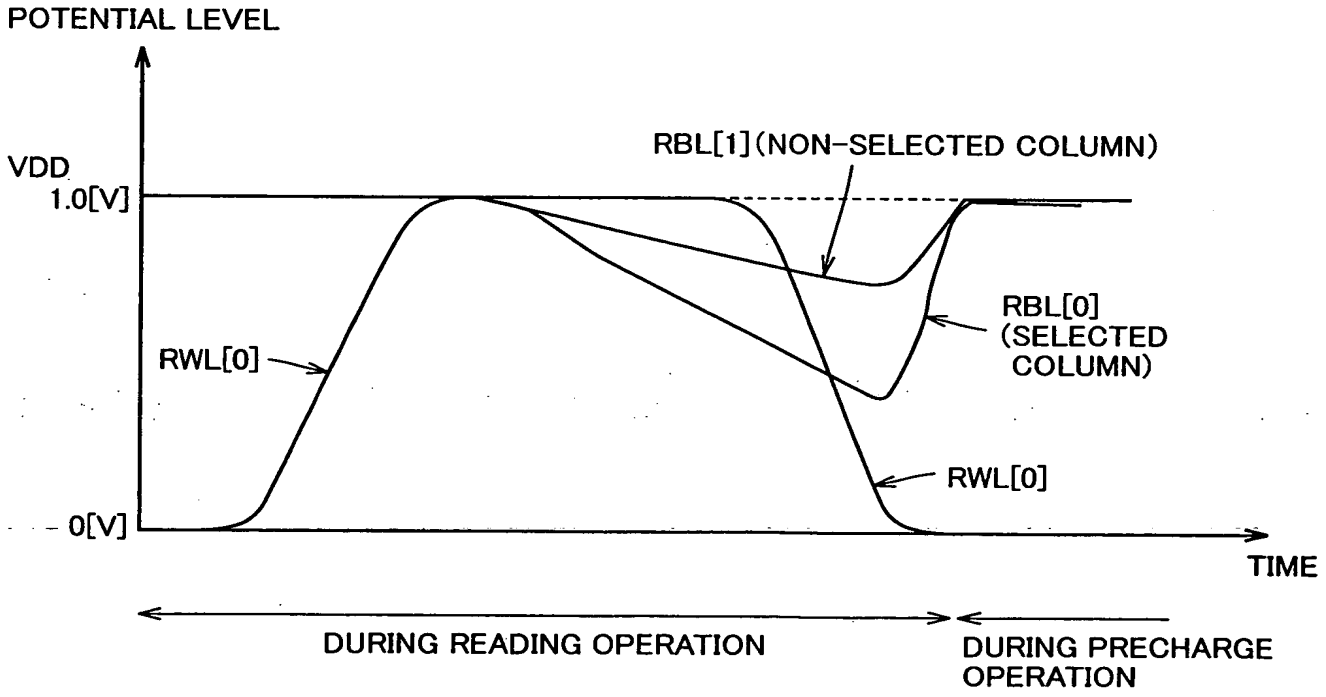
POTENTIAL LEVEL
VDD
1.0[V]
0[V]
RBL[1](NON-SELECTED COLUMN)
RBL[0] (SELECTED COLUMN)
RWL[0]
RWL[0]
TIME
DURING READING OPERATION
DURING PRECHARGE OPERATION

FIG.8

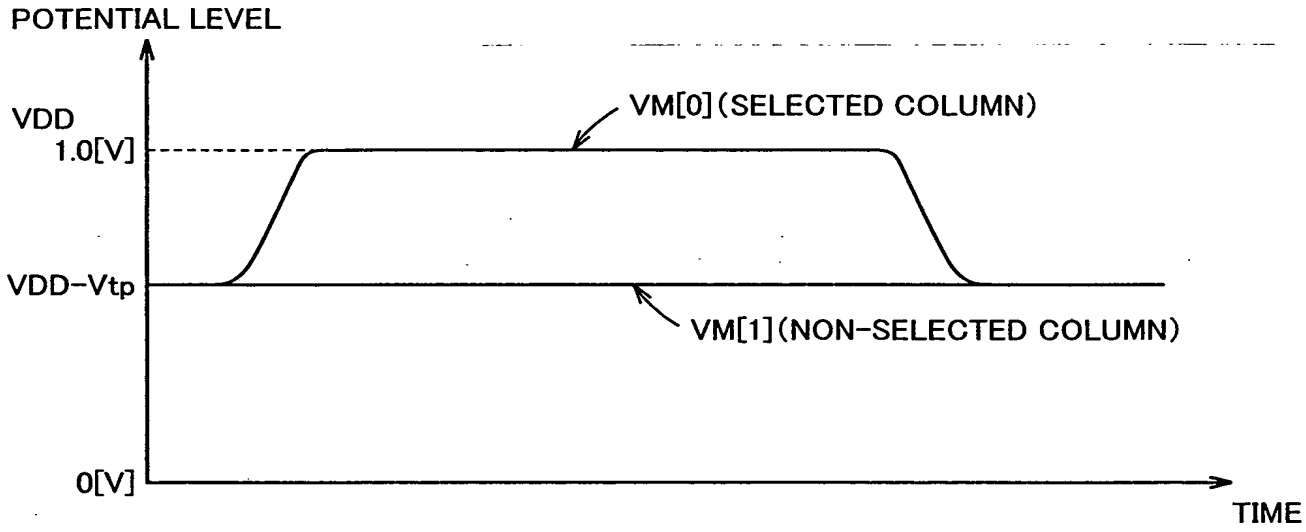
POTENTIAL LEVEL
VDD
1.0[V]
VDD-Vtp
0[V]
VM[0](SELECTED COLUMN)
VM[1](NON-SELECTED COLUMN)
TIME

FIG.9

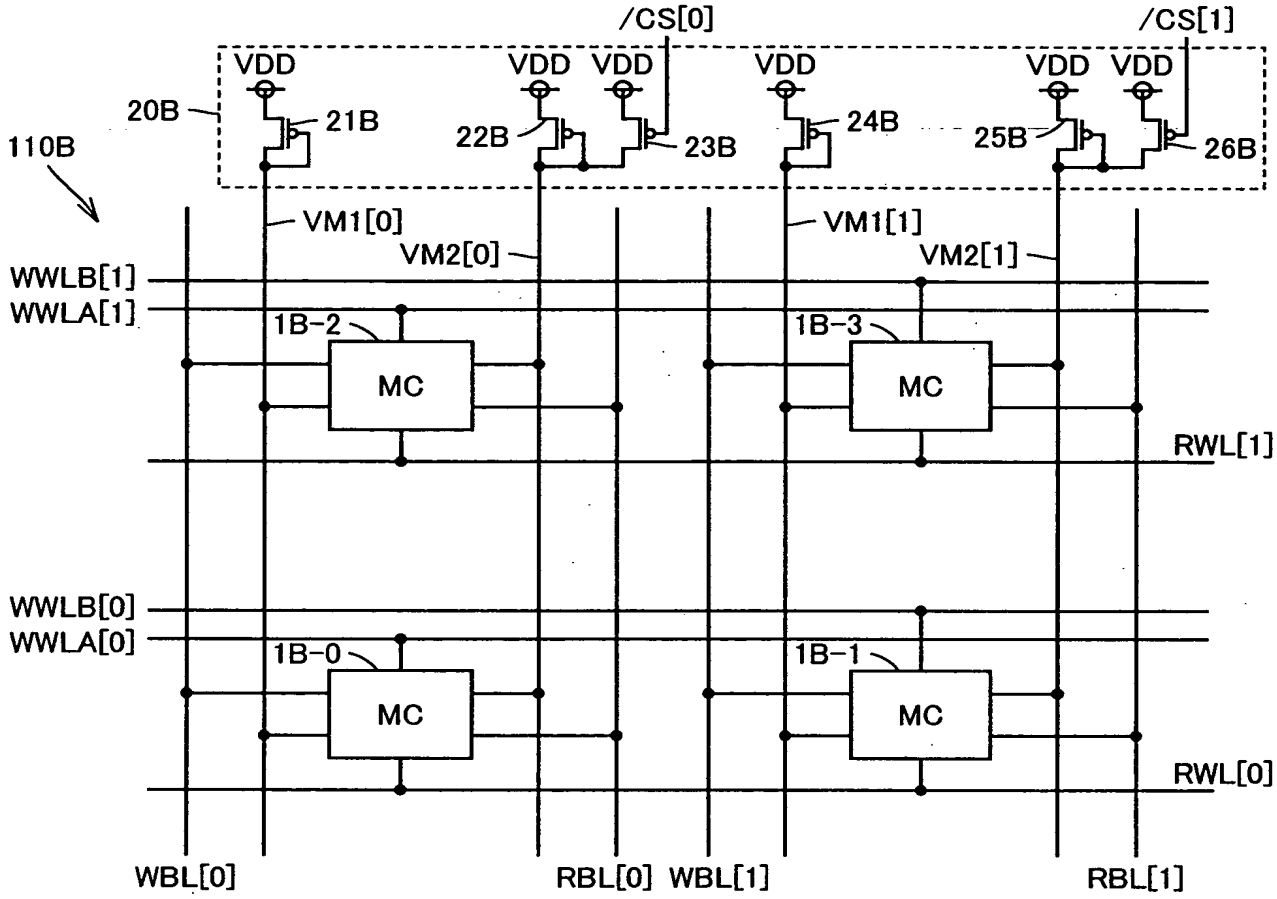
/CS[0]
/CS[1]
VDD
20B
21B
22B
23B
24B
25B
26B
110B
VM1[0]
VM2[0]
VM1[1]
VM2[1]
WWLB[1]
WWLA[1]
1B-2
1B-3
MC
RWL[1]
WWLB[0]
WWLA[0]
1B-0
1B-1
RWL[0]
WBL[0]
RBL[0]
WBL[1]
RBL[1]

FIG.10

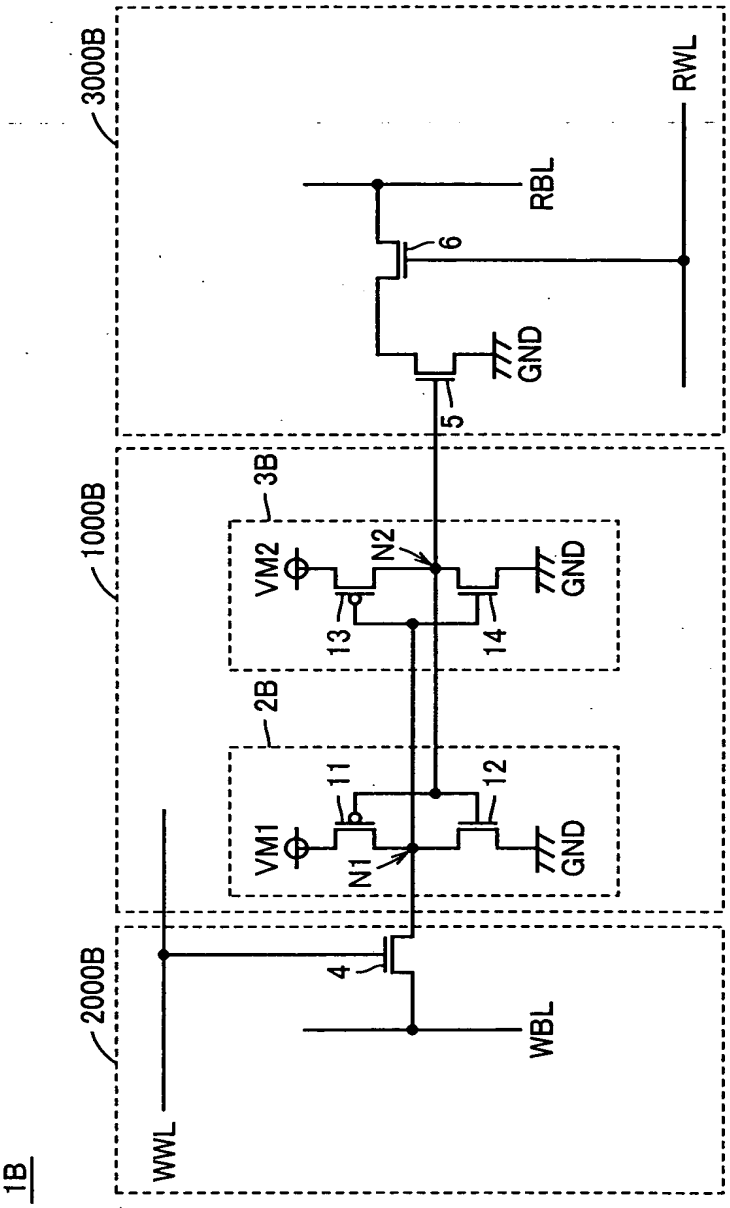
1B
3000B
1000B
2000B
3B
2B
RWL
RBL
WBL
WWL
GND
VM2
VM1
N2
N1
4
5
6
11
12
13
14

FIG.11

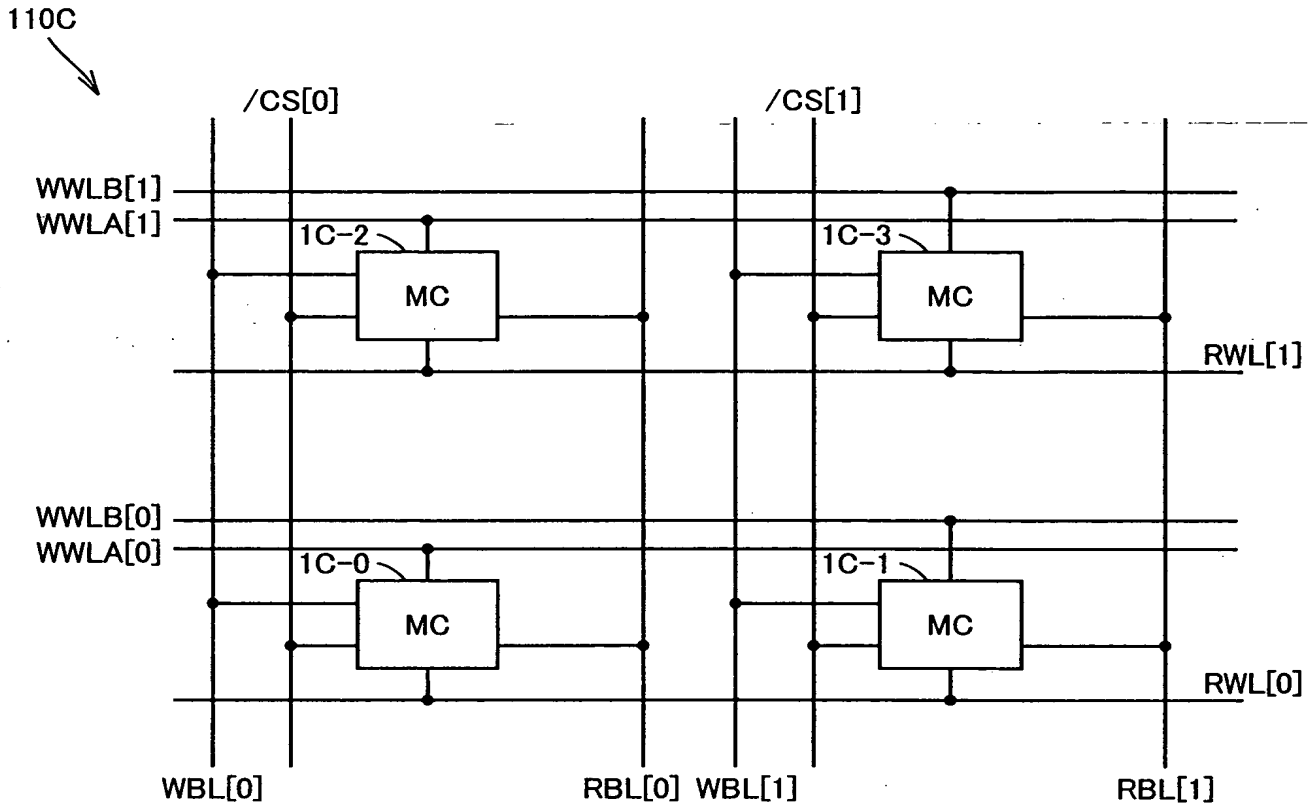
110C
/CS[0]
/CS[1]
WWLB[1]
WWLA[1]
1C-2
MC
1C-3
MC
RWL[1]
WWLB[0]
WWLA[0]
1C-0
MC
1C-1
MC
RWL[0]
WBL[0]
RBL[0]
WBL[1]
RBL[1]

FIG.12

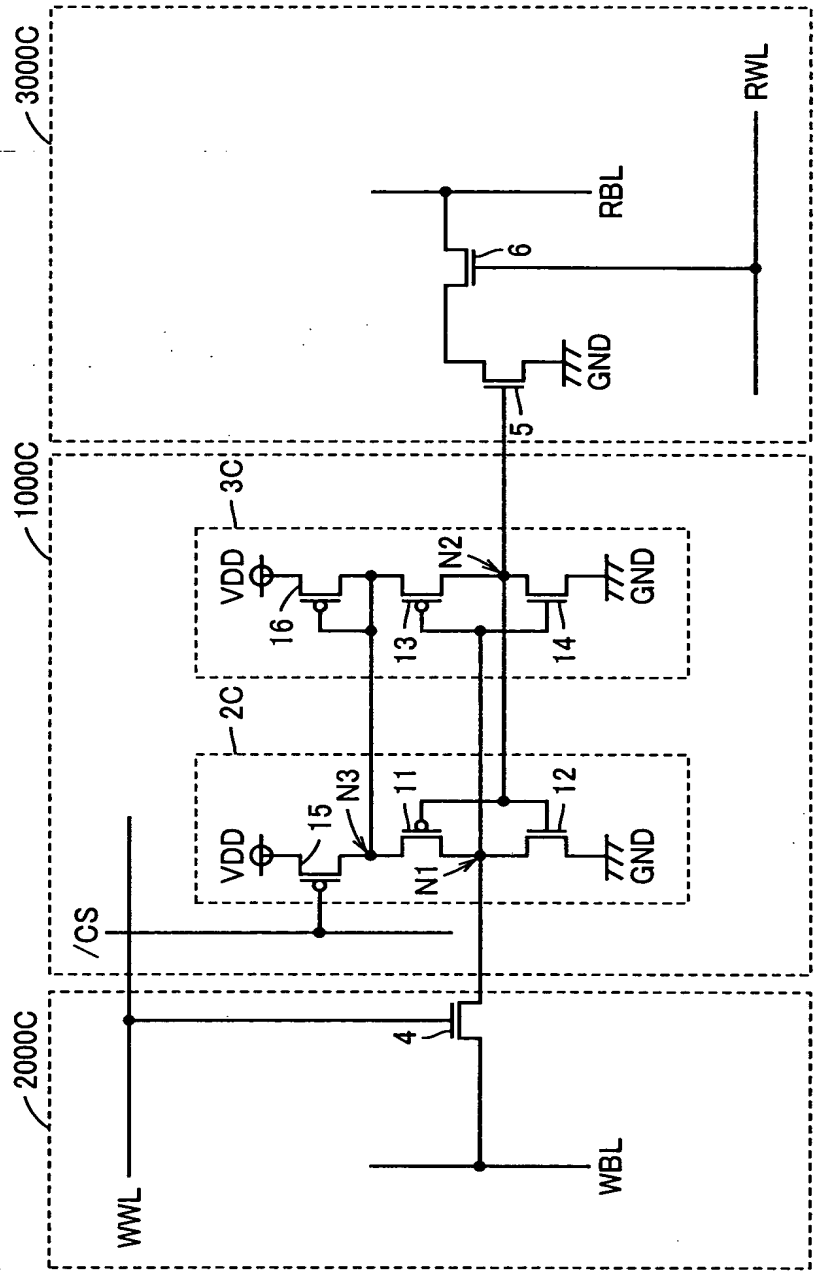
1C
3000C
1000C
2000C
3C
2C
RWL
RBL
6
GND
5
VDD
16
13
N2
14
GND
VDD
15
N3
11
12
N1
GND
/CS
4
WWL
WBL

FIG.13

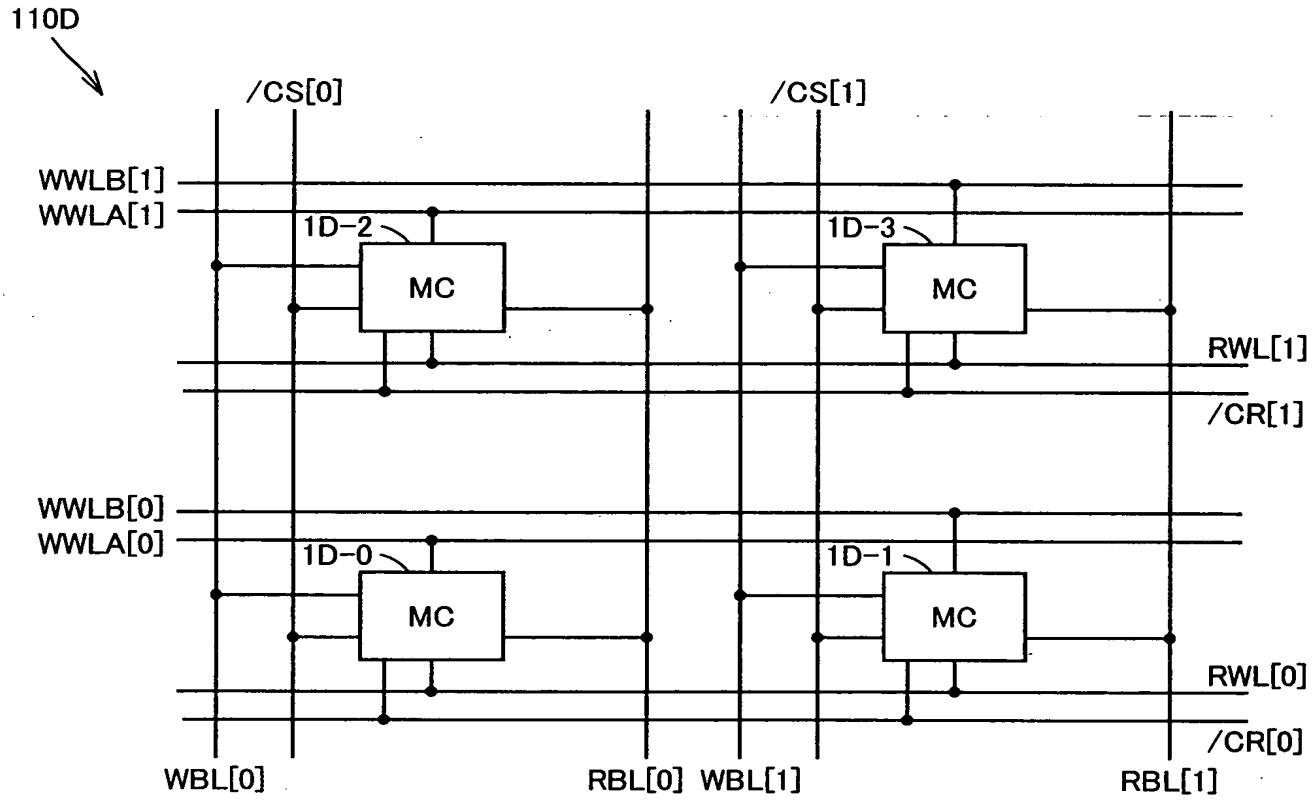
110D
/CS[0]
/CS[1]
WWLB[1]
WWLA[1]
1D-2
MC
1D-3
MC
RWL[1]
/CR[1]
WWLB[0]
WWLA[0]
1D-0
MC
1D-1
MC
RWL[0]
/CR[0]
WBL[0]
RBL[0]
WBL[1]
RBL[1]

FIG.14

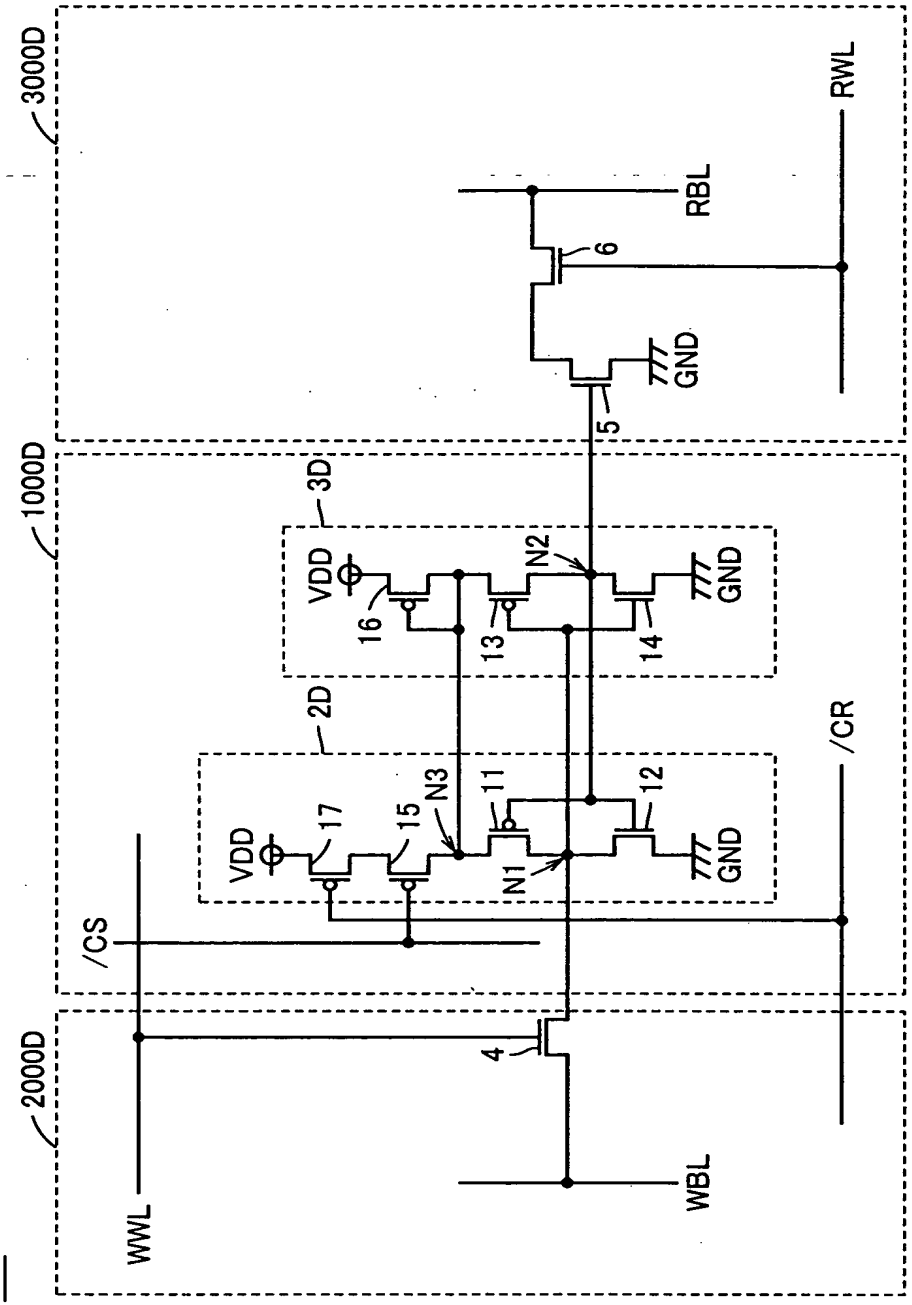
1D
3000D
1000D
2000D
RWL
RBL
6
GND
5
3D
VDD
N2
16
13
14
GND
2D
VDD
17
15
N3
11
12
GND
N1
/CS
/CR
4
WWL
WBL

FIG.15

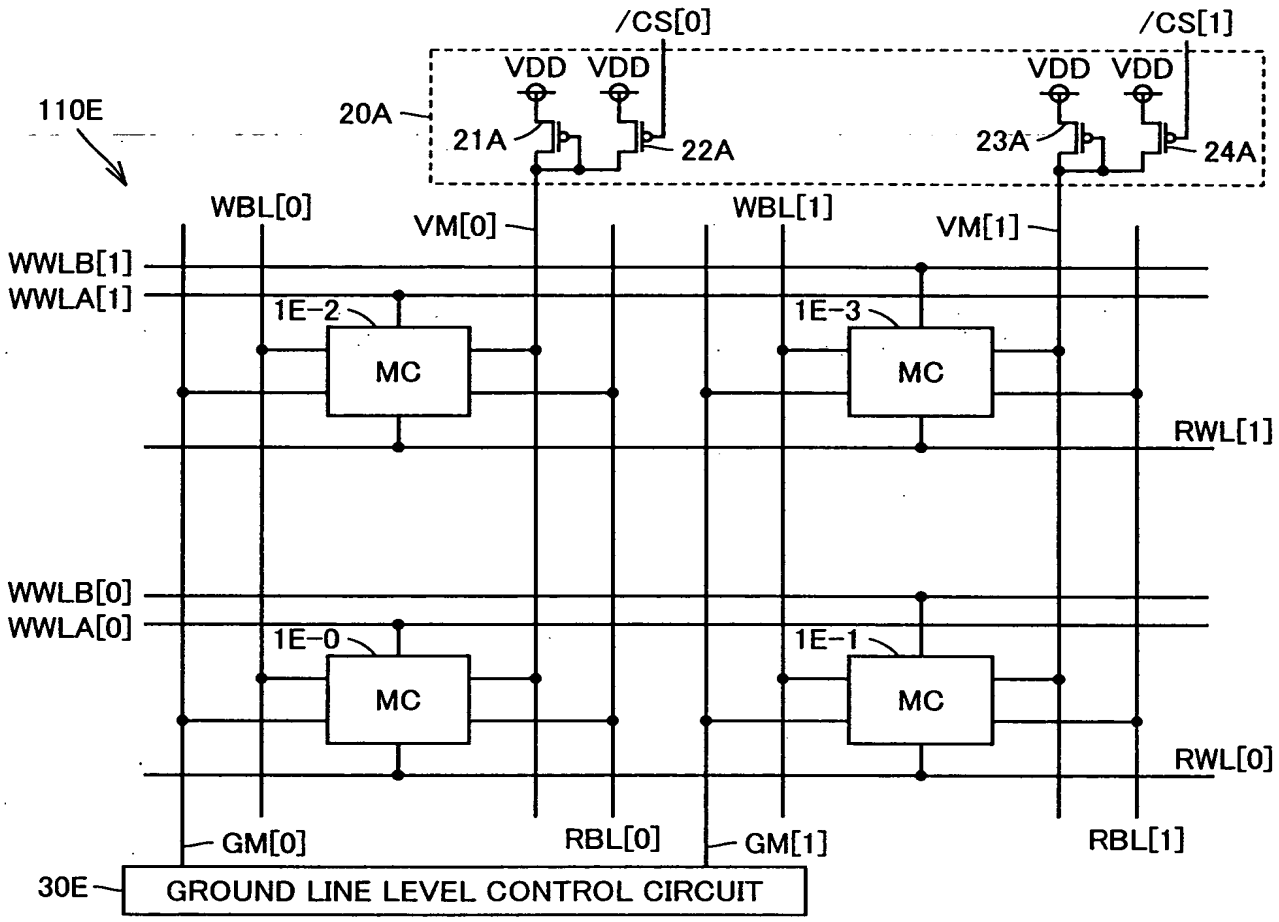
/CS[0]
/CS[1]
VDD
VDD
VDD
VDD
110E
20A
21A
22A
23A
24A
WBL[0]
VM[0]
WBL[1]
VM[1]
WWLB[1]
WWLA[1]
1E-2
MC
1E-3
MC
RWL[1]
WWLB[0]
WWLA[0]
1E-0
MC
1E-1
MC
RWL[0]
GM[0]
RBL[0]
GM[1]
RBL[1]
30E
GROUND LINE LEVEL CONTROL CIRCUIT

FIG.16

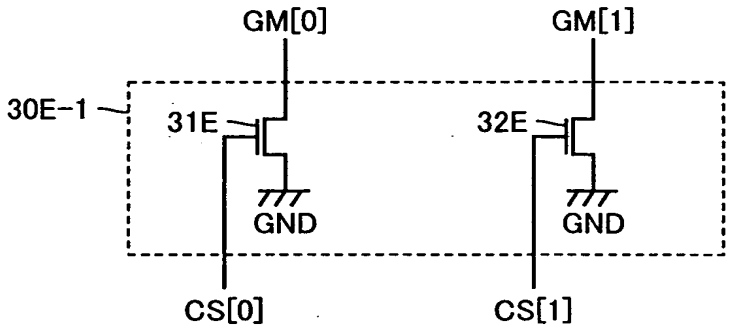
GM[0]
GM[1]
30E-1
31E
32E
GND
GND
CS[0]
CS[1]

FIG.17

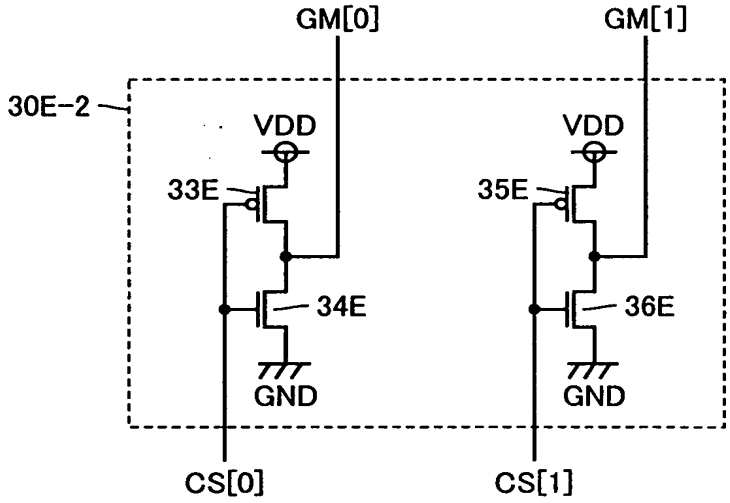
GM[0]
GM[1]
30E-2
VDD
VDD
33E
35E
34E
36E
GND
GND
CS[0]
CS[1]

FIG.18

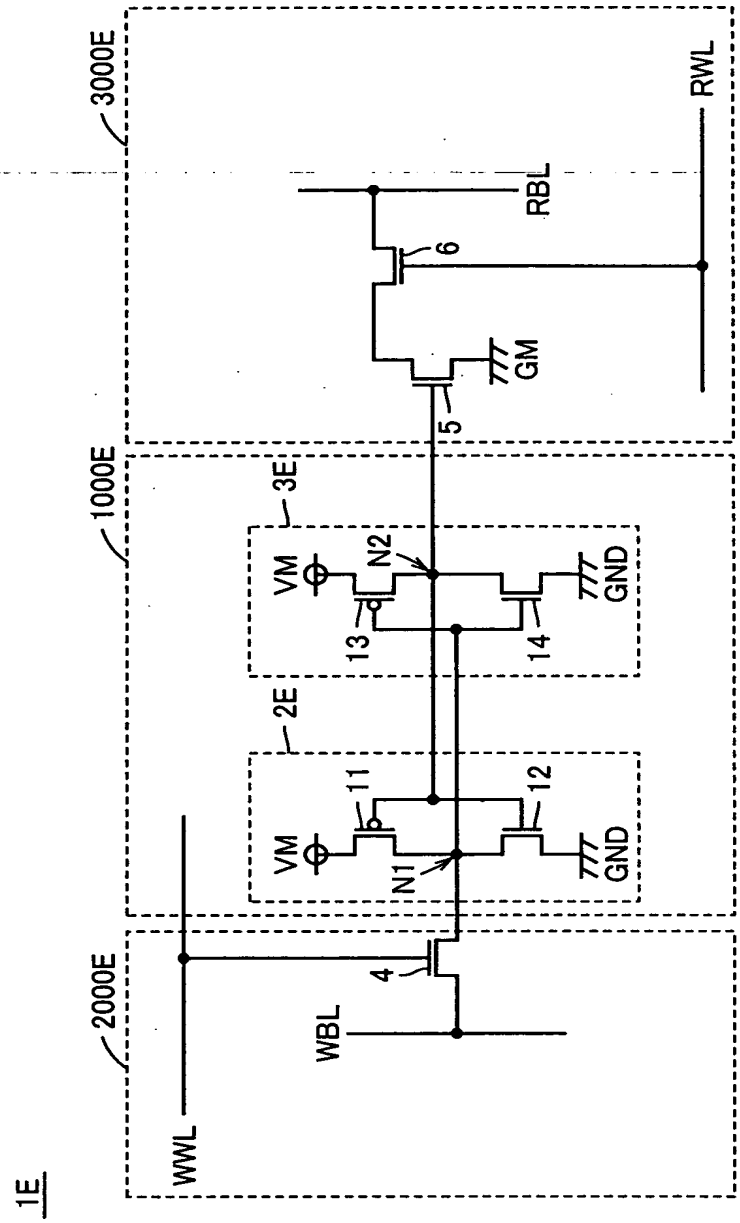
1E
3000E
1000E
2000E
3E
2E
RWL
RBL
6
GM
5
VM
N2
GND
13
14
11
12
N1
4
WBL
WWL

FIG.19

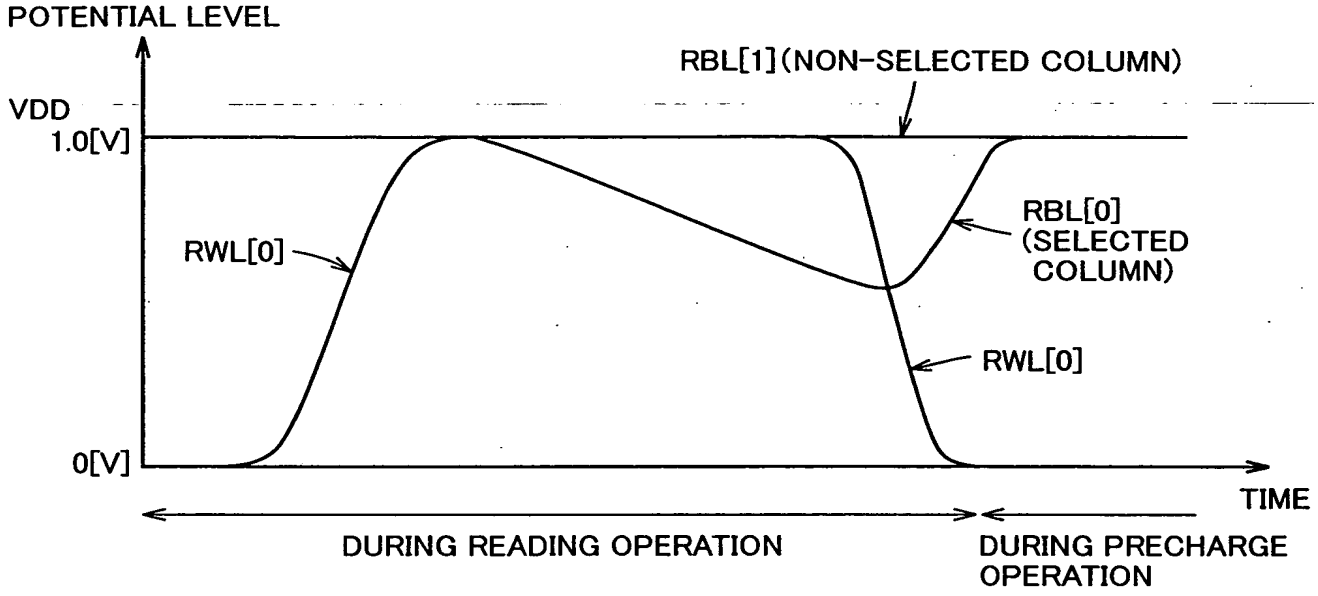
POTENTIAL LEVEL
RBL[1](NON-SELECTED COLUMN)
VDD
1.0[V]
RWL[0]
RBL[0]
(SELECTED
COLUMN)
RWL[0]
0[V]
TIME
DURING READING OPERATION
DURING PRECHARGE
OPERATION

FIG.20

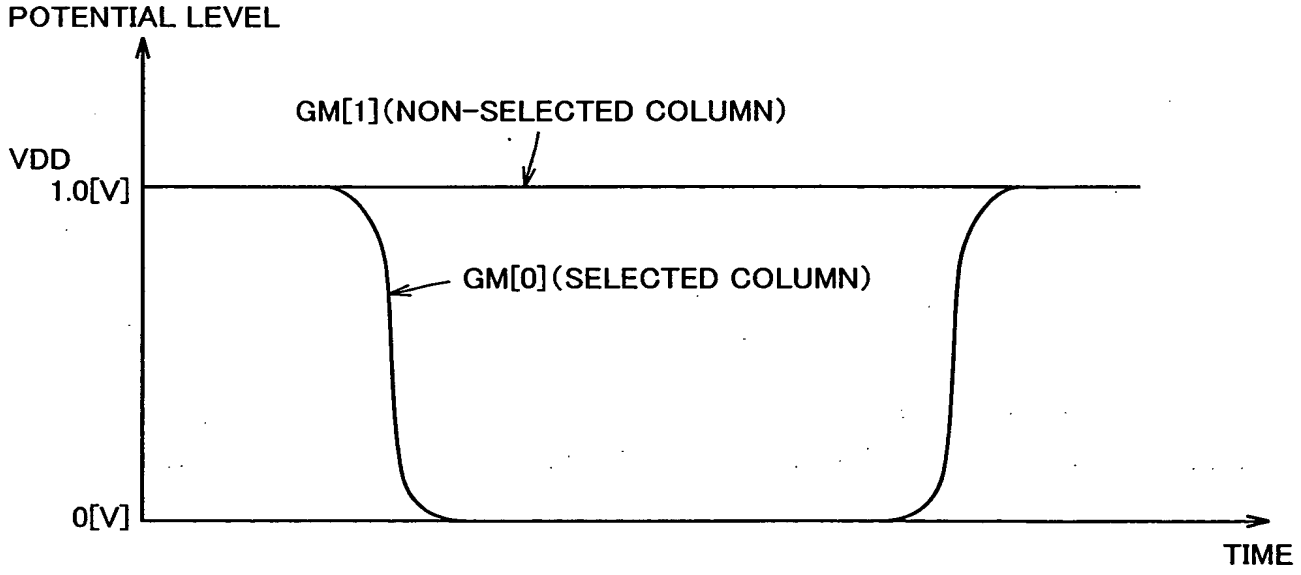
POTENTIAL LEVEL
GM[1](NON-SELECTED COLUMN)
VDD
1.0[V]
GM[0](SELECTED COLUMN)
0[V]
TIME

FIG.21

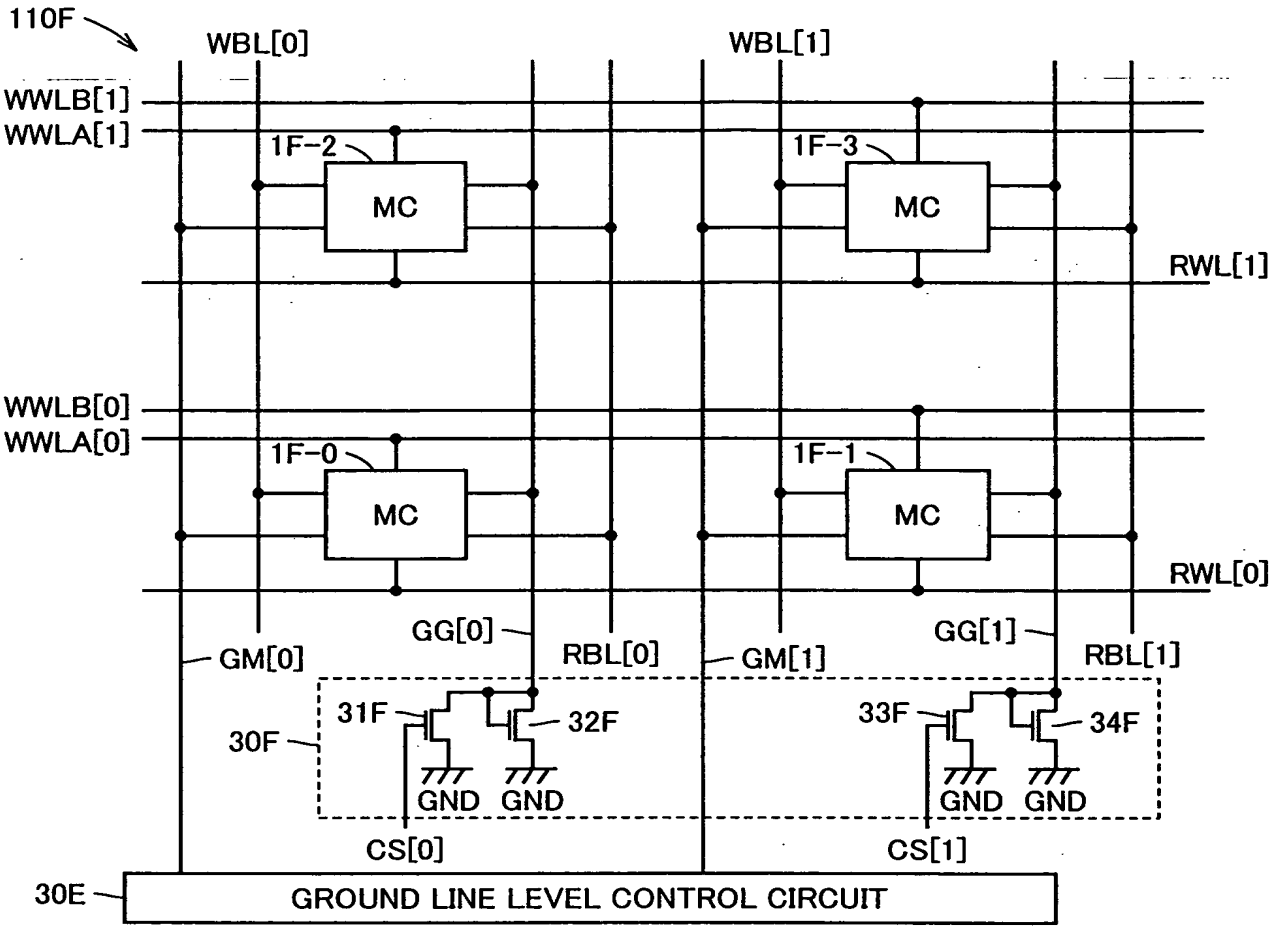
110F
WBL[0]
WBL[1]
WWLB[1]
WWLA[1]
1F-2
MC
1F-3
MC
RWL[1]
WWLB[0]
WWLA[0]
1F-0
MC
1F-1
MC
RWL[0]
GG[0]
GM[0]
RBL[0]
GM[1]
GG[1]
RBL[1]
30F
31F
32F
33F
34F
GND
GND
GND
GND
CS[0]
CS[1]
30E
GROUND LINE LEVEL CONTROL CIRCUIT

FIG.22

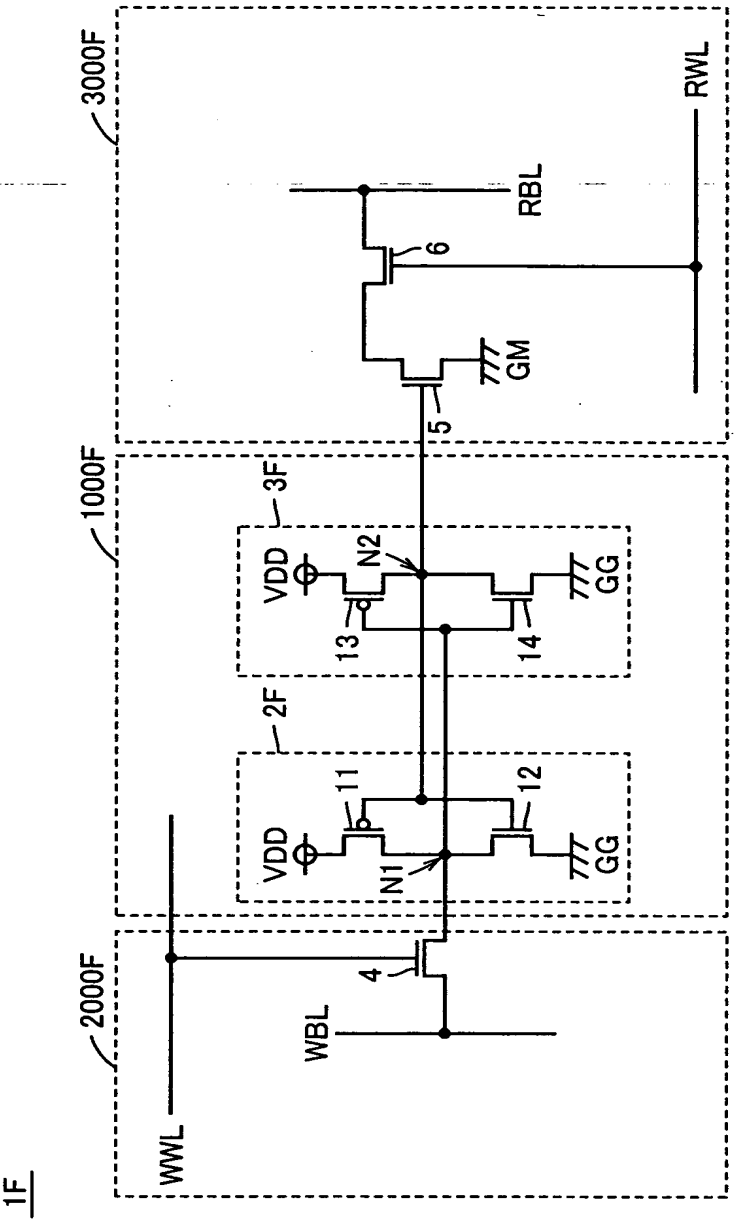
1F
3000F
1000F
2000F
3F
2F
RWL
RBL
6
GM
5
VDD
N2
13
14
GG
11
12
N1
4
WBL
WWL

FIG.23

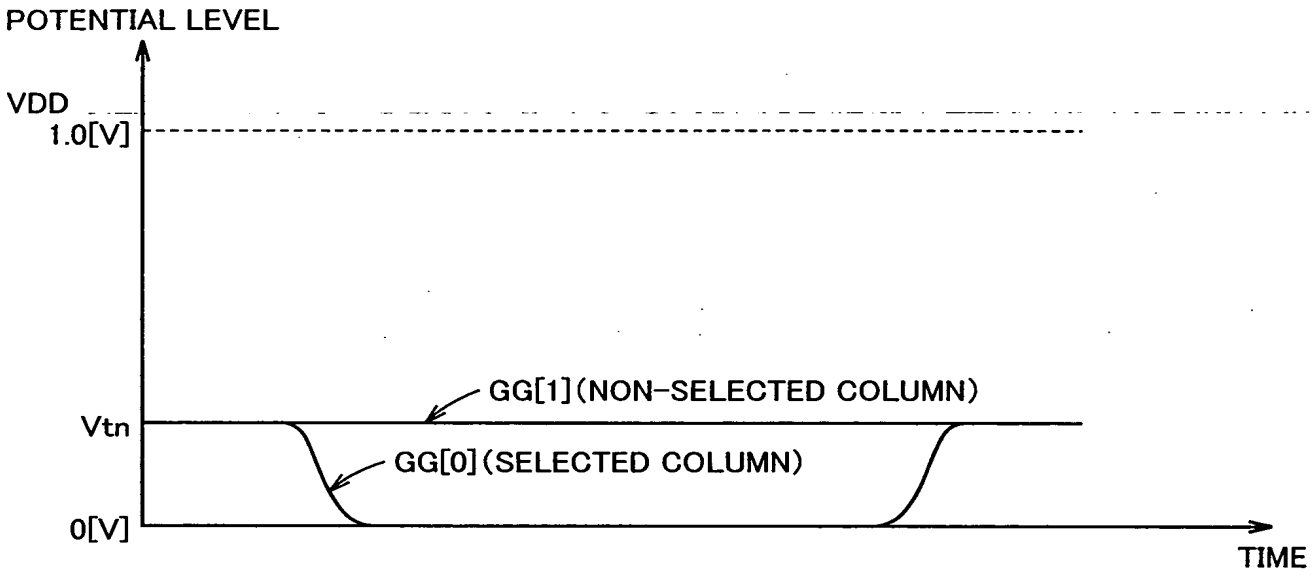
POTENTIAL LEVEL
VDD
1.0[V]
GG[1](NON-SELECTED COLUMN)
Vtn
GG[0](SELECTED COLUMN)
0[V]
TIME

FIG.24

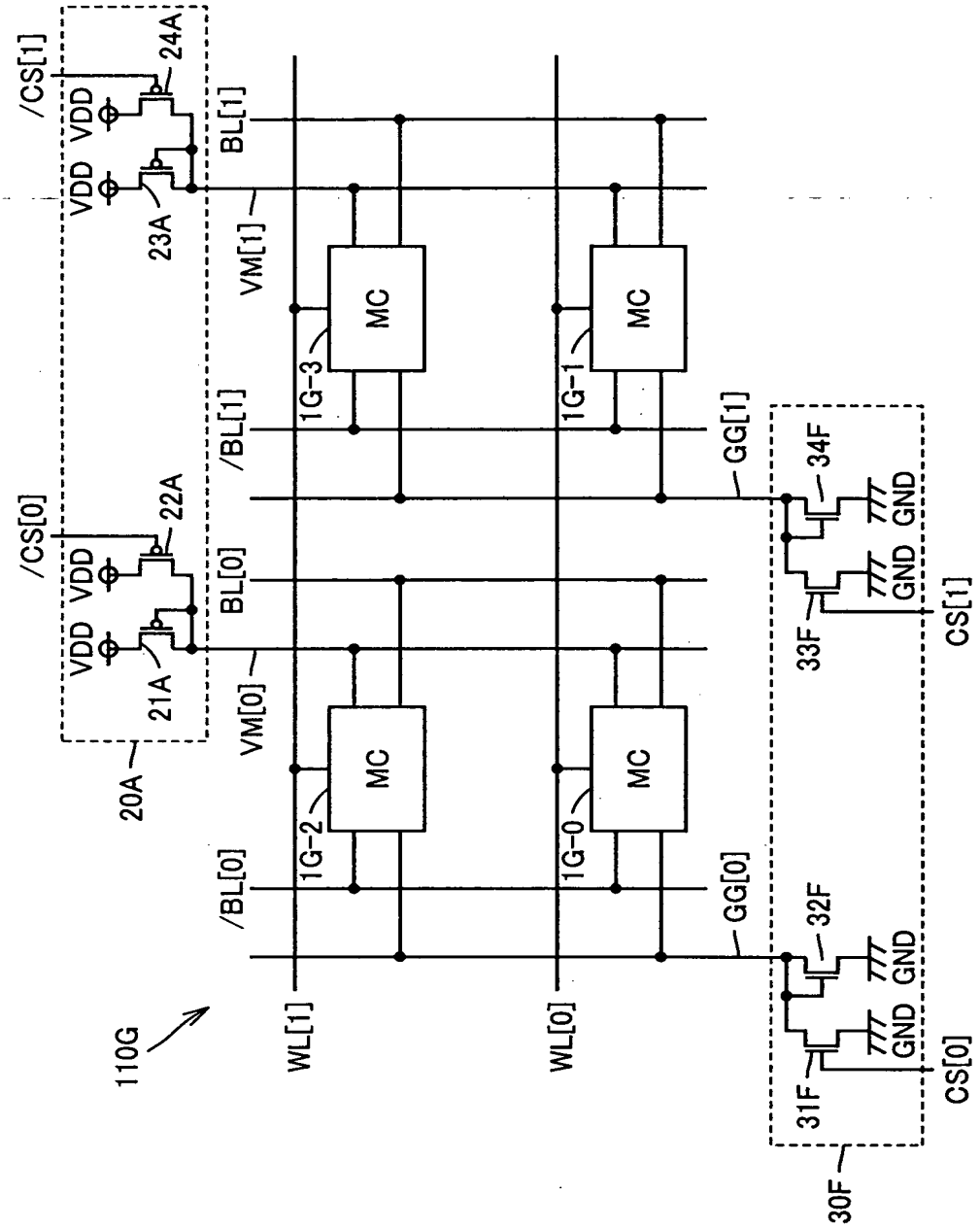
/CS[1]
/CS[0]
VDD
24A
23A
22A
21A
20A
BL[1]
BL[0]
/BL[1]
/BL[0]
VM[1]
VM[0]
MC
1G-3
1G-2
1G-1
1G-0
WL[1]
WL[0]
110G
GG[1]
GG[0]
34F
33F
32F
31F
30F
GND
CS[1]
CS[0]

FIG.25

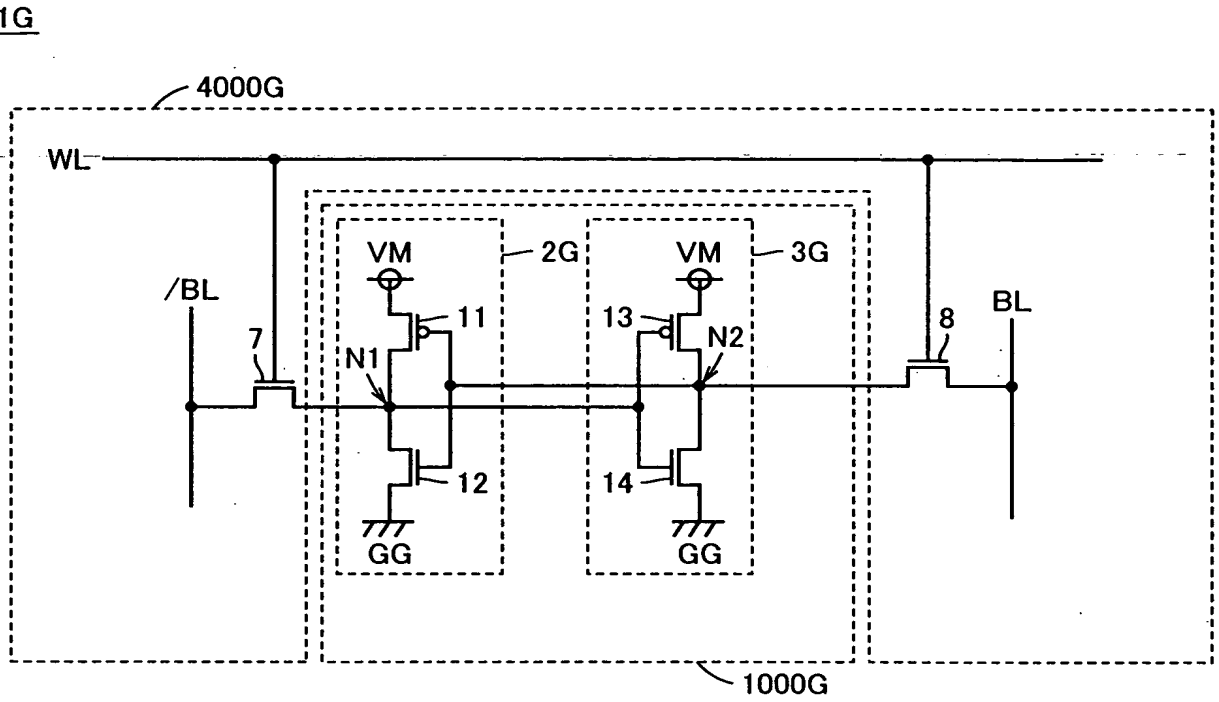
1G
4000G
WL
/BL
7
VM
2G
11
N1
12
GG
VM
3G
13
N2
14
GG
8
BL
1000G

FIG.26

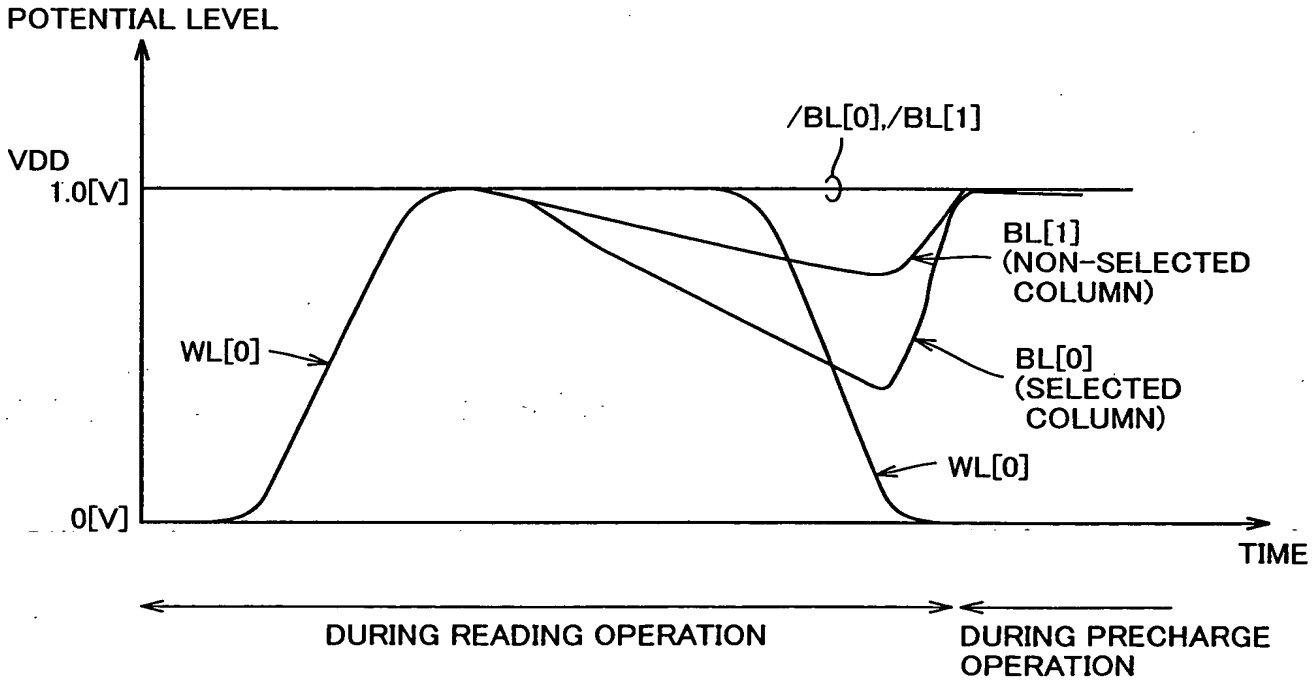
POTENTIAL LEVEL
VDD
1.0[V]
0[V]
/BL[0],/BL[1]
BL[1]
(NON-SELECTED
COLUMN)
WL[0]
BL[0]
(SELECTED
COLUMN)
WL[0]
TIME
DURING READING OPERATION
DURING PRECHARGE
OPERATION

FIG.27

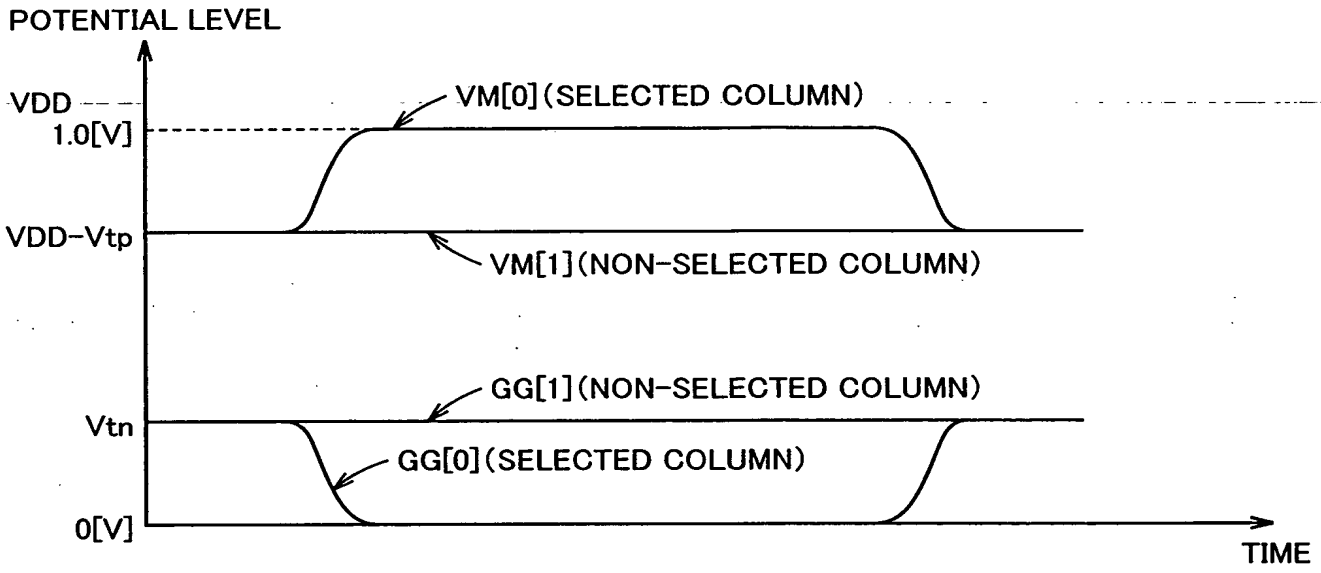
POTENTIAL LEVEL
VDD
1.0[V]
VDD-Vtp
Vtn
0[V]
VM[0](SELECTED COLUMN)
VM[1](NON-SELECTED COLUMN)
GG[1](NON-SELECTED COLUMN)
GG[0](SELECTED COLUMN)
TIME

FIG.28

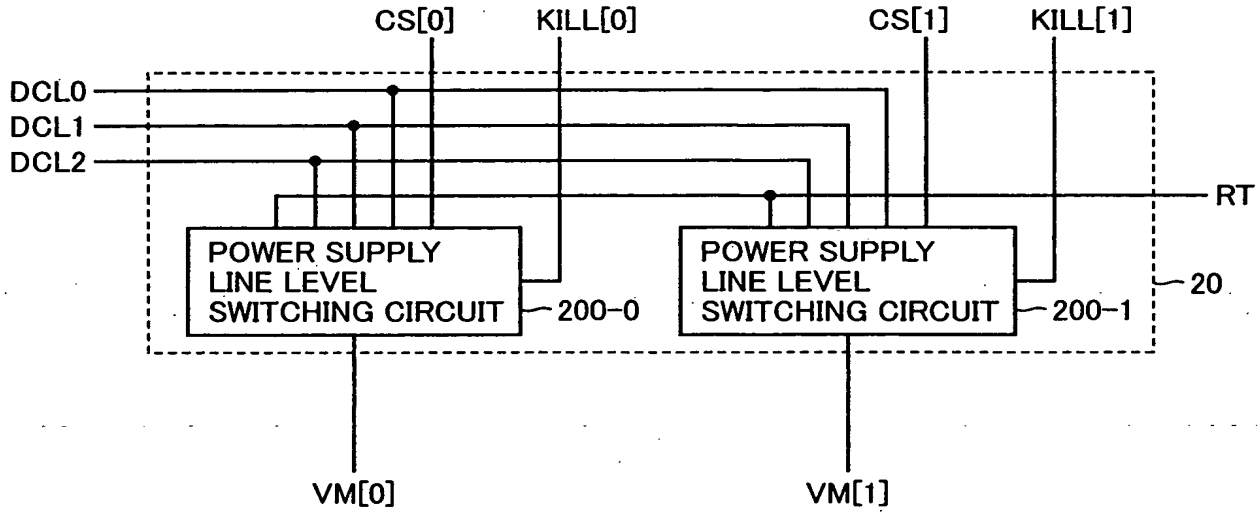
CS[0]
KILL[0]
CS[1]
KILL[1]
DCL0
DCL1
DCL2
RT
POWER SUPPLY LINE LEVEL SWITCHING CIRCUIT
200-0
POWER SUPPLY LINE LEVEL SWITCHING CIRCUIT
200-1
20
VM[0]
VM[1]

FIG.29

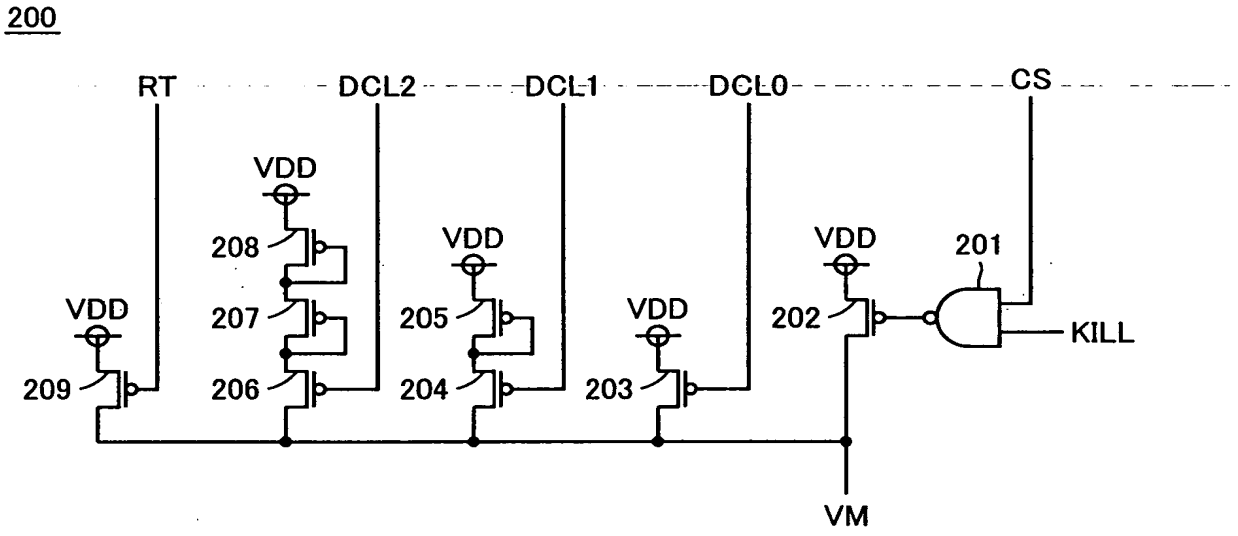
200
RT
DCL2
DCL1
DCL0
CS
VDD
208
207
206
VDD
209
VDD
205
204
VDD
203
VDD
202
201
KILL
VM

FIG.30

OPERATION MODE	RT	DCL2	DCL1	DCL0	CS	KILL	VM
DURING ACCESS	X	X	X	X	H	H	VDD
DURING NON-ACCESS	H	L	H	H	L	X	VDD-2Vtp
	H	H	L	H	L	X	VDD-Vtp
	H	H	H	L	L	X	VDD
DURING REDUNDANCY REPLACEMENT	H	H	H	H	X	L	Hi-Z
DURING RETENTION TEST	L	H	H	H	L	X	VDD

FIG.31

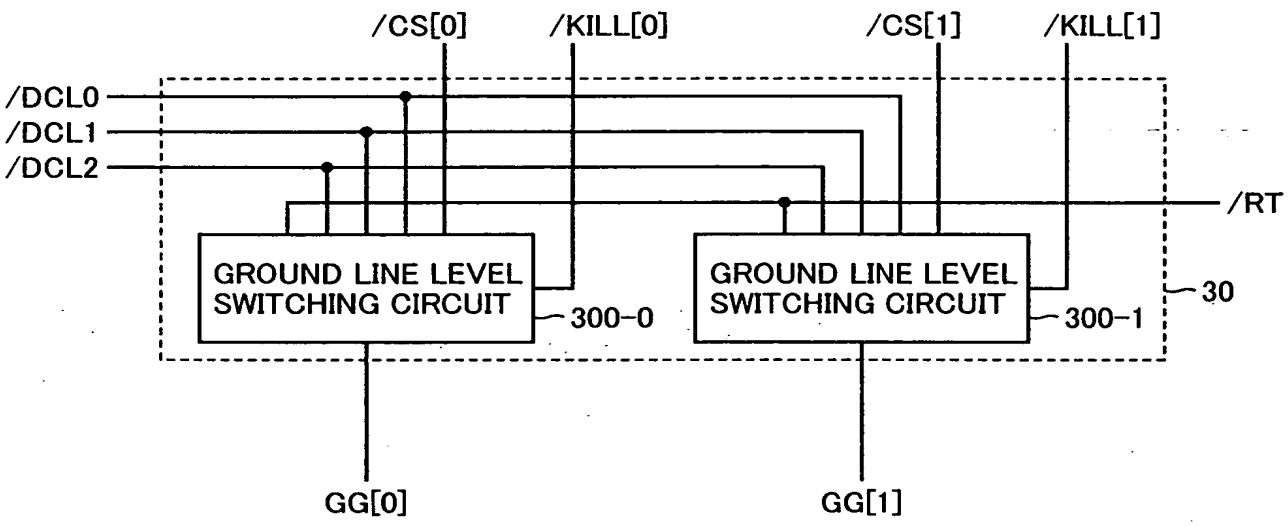
/CS[0]
/KILL[0]
/CS[1]
/KILL[1]
/DCL0
/DCL1
/DCL2
/RT
GROUND LINE LEVEL SWITCHING CIRCUIT
300-0
GROUND LINE LEVEL SWITCHING CIRCUIT
300-1
30
GG[0]
GG[1]

FIG.32

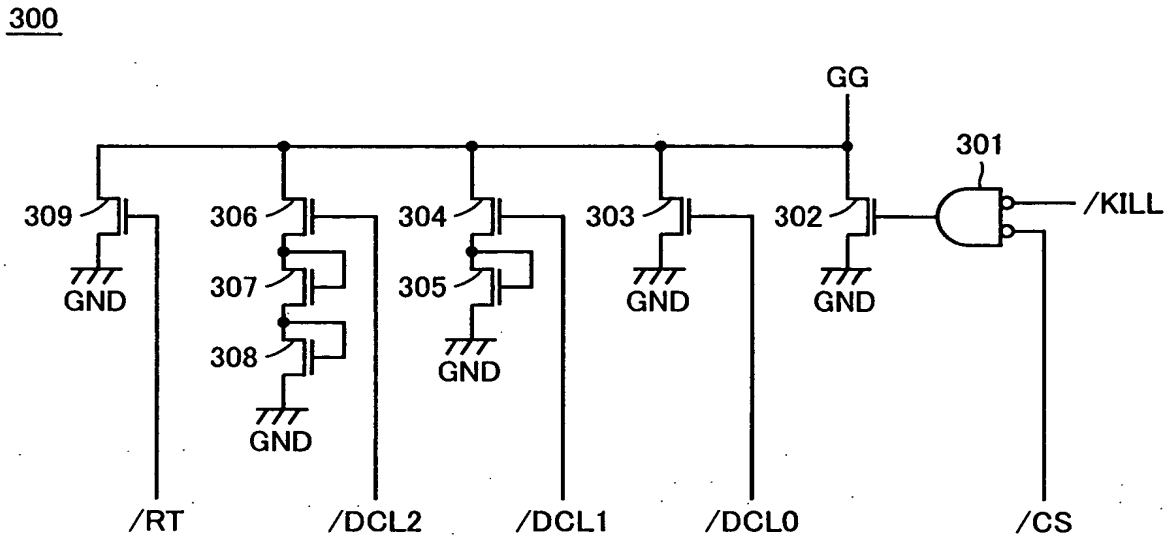
300
GG
301
309
306
304
303
302
/KILL
GND
307
305
GND
GND
GND
308
GND
/RT
/DCL2
/DCL1
/DCL0
/CS

FIG.33

OPERATION MODE	/RT	/DCL2	/DCL1	/DCL0	/CS	/KILL	GG
DURING ACCESS	X	X	X	X	L	L	GND
DURING NON-ACCESS	L	H	L	L	H	X	GND+2Vtn
	L	L	H	L	H	X	GND+Vtn
	L	L	L	H	H	X	GND
DURING REDUNDANCY REPLACEMENT	L	L	L	L	X	H	Hi-Z
DURING RETENTION TEST	H	L	L	L	H	X	GND

FIG.34

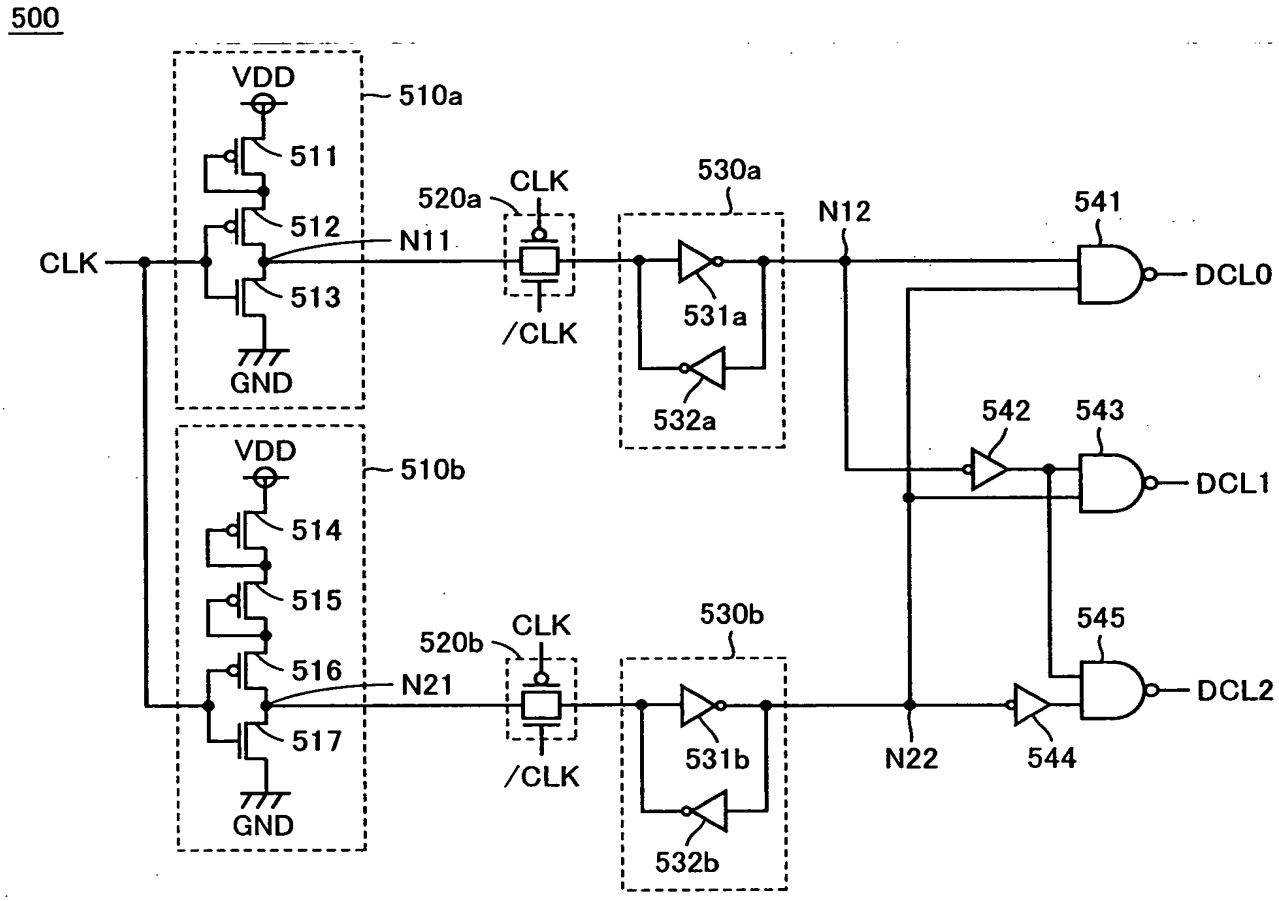
500
VDD
510a
511
512
513
GND
CLK
N11
520a
CLK
/CLK
530a
531a
532a
N12
541
DCL0
542
543
DCL1
VDD
510b
514
515
516
517
GND
N21
520b
CLK
/CLK
530b
531b
532b
N22
544
545
DCL2

FIG.35A

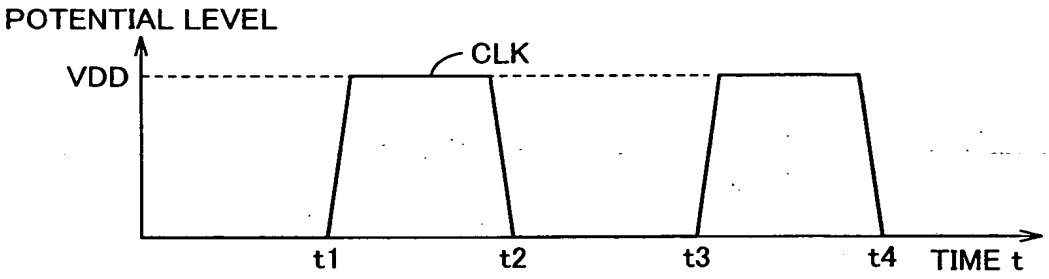

FIG.35B

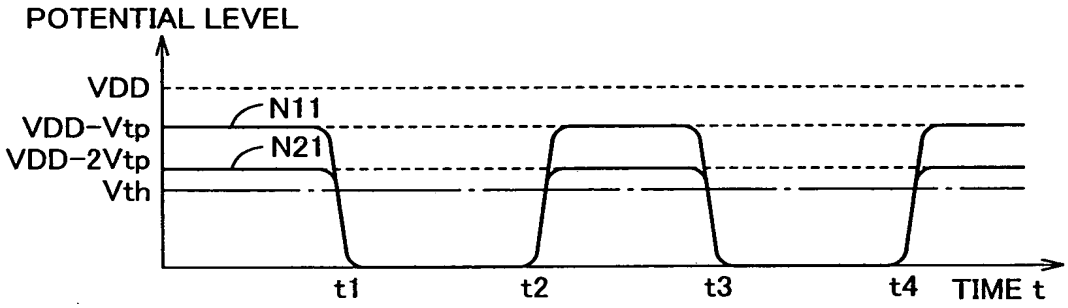

FIG.35C

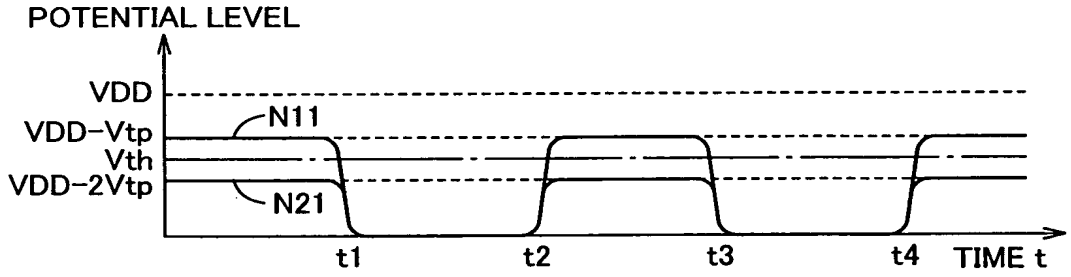

FIG.35D